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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,936	09/09/2003	Richard M. Fastow	AMD-H0561	3102

7590 01/23/2007

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EXAMINER	
NGUYEN, DAO H	
ART UNIT	PAPER NUMBER
2818	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,936	FASTOW ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,8,10,12,21-23 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8, 10, 12, 21-23 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 09/18/2006 through 10/31/2006.

Claims 1, 8, 10, 12, 21-23 and 25 are active in this application.

Claim(s) 2-7, 9, 11, 13-20 and 24 have been cancelled.

Remarks

2. Applicant's argument(s), filed 09/18/2006, have been fully considered, but are not totally persuasive. See the following rejection(s) for details.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim(s) 1, 8, 10, 12, 21-23 and 25 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,348,380 to Weimer et al.

Regarding claim 1, Weimer discloses a flash memory cell, as shown in figs. 9-10, comprising:

a substrate 220 comprising a source and a drain;

a silicon dioxide layer (silicon oxide layer formed by thermal oxidation at the interface between Ta_2O_5 layer 230 and silicon substrate 220: oxide-silicon interface; col. 10, lines 1-22) adjoining said substrate 220;

a dielectric layer 230 adjoining said silicon dioxide layer, said dielectric layer 230 comprising a dielectric material having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide (Ta_2O_5);

a polysilicon floating gate 250 adjoining said dielectric layer 230;

an oxide-nitride-oxide (ONO) layer 260 adjoining said floating gate 250; and

a control gate 270 adjoining said ONO layer 260, wherein said substrate 220, said silicon dioxide layer (thermal oxide layer), said dielectric layer 230, said floating gate 250, said ONO layer 260 and said control gate 270 are arranged in a laminate structure, wherein said silicon dioxide layer is sandwiched between said substrate 220 and said dielectric layer 230, wherein said dielectric layer 230 is sandwiched between said silicon dioxide layer and said floating gate 250, and wherein said ONO layer 260 is sandwiched between said floating gate 250 and said control gate 270.

Regarding claim 8, Weimer discloses the flash memory cell wherein said dielectric layer 230 comprises a composite of said metal oxide (Ta_2O_5) and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate (the dielectric layer 230 also comprise silicon oxide material formed by thermal oxidation at the interface between Ta_2O_5 layer 230 and silicon floating gate 250: oxide-silicon interface; col. 10, lines 1-22).

Regarding claim 10, Weimer discloses a flash memory array, as shown in figs. 9-10, comprising memory cells, wherein a memory cell comprises:

a substrate 220 comprising a source and a drain;

a tunnel oxide layer 230 adjoining said substrate 220, said tunnel oxide layer 230 comprising a dielectric material having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide (Ta_2O_5);

a first layer comprising a silicon material (silicon oxide layer formed by thermal oxidation at the interface between Ta_2O_5 layer 230 and silicon floating gate 250: oxide-silicon interface; col. 10, lines 1-22);

a polysilicon floating gate 250 adjoining said first layer;

an oxide-nitride-oxide (ONO) layer 260 adjoining said floating gate 250; and

a control gate 270 adjoining said ONO layer 260, wherein said substrate 220, said tunnel oxide layer 230, said first layer, said floating gate 250, said ONO layer 260 and said control gate 270 are arranged in a laminate structure, wherein said tunnel oxide layer 230 is sandwiched between said substrate 220 and said first layer (thermal

oxide layer)1, wherein said first layer is sandwiched between said tunnel oxide layer 230 and said floating gate 250, and wherein said ONO layer 260 is sandwiched between said floating gate 250 and said control gate 270.

Regarding claim 12, Weimer discloses the flash memory array wherein said silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. col. 10, lines 1-22.

Regarding claim 21, Weimer discloses a flash memory cell, as shown in figs. 9-10, comprising:

a substrate 220 comprising a source and a drain (col. 12, lines 31-33);

a first layer comprising a first silicon material (silicon oxide layer formed by thermal oxidation at the interface between Ta_2O_5 layer 230 and silicon substrate 220: oxide-silicon interface; col. 10, lines 1-22) and adjoining said substrate 220;

a dielectric layer 230 adjoining said first layer, said dielectric layer 230 comprising a dielectric material having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide (Ta_2O_5; col. 6, lines 24-33);

a second layer comprising a second silicon material (silicon oxide layer formed by thermal oxidation at the interface between Ta_2O_5 layer 230 and silicon floating gate 250: oxide-silicon interface; col. 10, lines 1-22) and adjoining said dielectric layer 230;

a polysilicon floating gate 250 adjoining said second layer;

an oxide-nitride-oxide (ONO) layer 260 adjoining said floating gate 250; and

a control gate 270 adjoining said ONO layer 260, wherein said substrate 220, said first layer, said dielectric layer 230, said second layer, said floating gate 250, said ONO layer 260 and said control gate 270 are arranged in a laminate structure, wherein said first layer is sandwiched between said substrate 220 and said dielectric layer 230, wherein said dielectric layer 230 is sandwiched between said first layer and said second layer, wherein said second layer is sandwiched between said dielectric layer 230 and said floating gate 250, and wherein said ONO layer 260 is sandwiched between said floating gate 250 and said control gate 270.

Regarding claim 22, Weimer discloses the flash memory cell wherein said first silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 10, lines 1-22.

Regarding claim 23, Weimer discloses the flash memory cell wherein said second silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 10, lines 1-22.

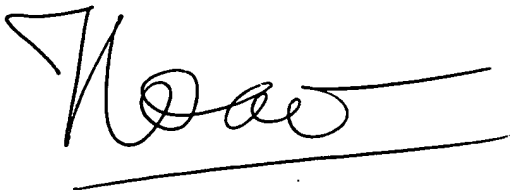
Regarding claim 25, Weimer discloses the flash memory cell wherein said dielectric layer 230 comprises a composite of said a metal oxide (Ta_2O_5) and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See 6, lines 24-39.

Conclusion

5. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571)272-1907. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.



Dao H. Nguyen
Art Unit 2818
January 03, 2007